CIRCUIT OVERVIEW

AC IN

Three line chokes in series and capacitors across the outputs are used to provide Line Conducted Interference (LCI) suppression to the AC line. A full wave bridge is connected to the 60Hz ac line to provide Raw B+ to both the standby Zero Voltage Switching (ZVS) circuit and the main high power isolating regulator.

A provision for a Negative Temperature Coefficient Resistor (NTC) RT14202 may be used as a surge current resistor to control inrush current through the diodes as the main electrolytic charges initially to minimize power and temperature.

Grounding of the 3-wire line cord is to the metal mechanical structure to which the main spark gap and audio/video grounds are connected

Main Run Power Supply Operation

The main run power supply circuit operates in the Zero Voltage Switching (ZVS) mode to minimize radiated noise and to improve efficiency.

A high power output, single switch power supply requires a switching device that has a high current rating and high breakdown voltage. The most cost-effective type of device for this application is a bipolar switching transistor, but bipolar transistor require a significant amount of base current drive in the forward direction, and even higher level of current during turn-off to ensure fast switching.

A simple proportional drive circuit that also provides a self-oscillating capability has been developed for the CTC210. Proportional drive is advantageous because it provides a relatively constant ratio of base current to collector current. This constant ratio prevents the switching transistor base from being overdriven in the forward direction during low current operation, thus improving the switching speeds. Proportional drive also provides increased base drive when high peak current is required from the switching transistor to ensure proper saturation to minimize power dissipation. This circuit operates in the forward mode because of the high power output requirements, providing energy to the secondary windings during the main switch conduction interval. In this implementation the primary winding of T14101, provides the means for the energy stored in the resonant inductor to be transferred to the output while the switching transistor is on.

A high current latch provides a low impedance path for reverse base current to flow during turn-off. The latch is made up of Q14101 and Q14103 a PNP/NPN transistor pair. A negative bias on the base of the switching transistor, Q14100, is provided by the drive transformer, a series Zener diode, CR14105, and bypass capacitor, C14103, to improve reliability and switching speeds.

Oscillation is initiated by current flowing from a high value resistor R14103 connected to the Raw B+. It causes a small amount of base current to flow in the main power switch Q14100. A drive transformer T14101 is connected as a current transformer and causes current to flow in the secondary winding in response to the current flow in the primary winding. The ratio of primary current to secondary current is determined by the turns ratio of the drive transformer, about 7 to 1. Since additional current begins to flow in the base of the switching transistor from the secondary of T14101, additional current will flow in the primary and a regenerative effect will take place causing the system to self oscillate. The expected range of switching frequency is 80kHz to 120 kHz.

Switch Mode transistor current is sensed by an emitter resistor, R14100; the developed voltage is fed to the NPN/PNP latch. When the voltage across R14100 increases the base of Q14103 becomes sufficiently positive to cause it to turn-on. Current flowing in Q14103 causes Q14101 to turn-on diverting base current away from the Q14100 and latching Q14103. CR14105 and C14103 provide a negative voltage feedback to the base of Q14100 to improve the turn off characteristics of the main power switch.

Diode CR14108 and resistor R14117 shunt some of the reverse base current to the low impedance of the current sense resistor. This shunting effect prevents the overstressing the base of Q14103.

Q14102 and Q14103 remain latched until the current flowing through the pair drops below the latching threshold. The negative voltage produced by T14101 keeps the main switch mode transistor from conducting until the resonant action of the resonating inductor and the resonant capacitor, C14113, causes the voltage to reverse. As the voltage at the base of Q14100 rises, current begins to flow and the next cycle begins.

When Q14100 turns off, the collector voltage begins to rise but the voltage change is limited by the resonance effect produced by L14103 and C14113. Because Q14100 turns off very rapidly, very little power is dissipated since the collector voltage remains low during the turn-off interval. When the collector voltage of Q14100 resonates toward ground, the collector-base junction conducts and diode CR14128 provides a path for the resonant current returning to the Raw B+ supply after the resonant cycle is complete. Diode CR14115 provides a current path of the forward drive current and limits the voltage to which C14104 can charge. A negative base bias voltage is coupled to Q14100 through C14104 to Q14100 when it is in the off state. Diode CR14117 and C14121 bias and rectify and filter the negative voltage

developed from the drive transformer, T14101, to provide a negative supply voltage for the control circuit.

A feedback signal from an error amplifier that senses the output voltage of the supply drives an opto-coupler with a variable current. The +76V supply is sensed via a resistor divider and fed to the reference IC U14101. As the output voltage increases above the threshold set by the error amplifier, the current through the diode portion of the opto-coupler increases causing increasing current to flow in the transistor portion. This increased current flow causes the voltage across C14112 to drop which in turn lowers the threshold at which Q14103 will begin to conduct, lowers the peak current in the switching device, and reduces the output voltage of the system until equilibrium is established.

Overcurrent Protection

When an overload appears, the current through (and the voltage across) the sense resistors approaches a sawtooth shape with nearly equal positive and negative amplitudes. The negative-going portion of this voltage is passed by CR14122 and lowers the voltage on the emitter of Q14103 that in turn lowers the maximum peak current that can flow through the transistor.

Standby Power Operation

The standby power supply uses a ZVS circuit similar to the main run circuitry. It uses a flyback topology rather than the forward mode of the main power supply. A MOSFET, Q14601, serves as the switching device with the energy storage components the primary inductance of T14600 and the resonating capacitor, C14605.

+5VFB is sampled and regulated directly via the reference IC U14603 and opto-coupler, U14601. A transistor switch Q14604 is enabled by the +12v run in order to shed load in the standby mode.

An isolated supply (+8V_USB) provides the source for the USB 5v regulator that is located on the I/O board. This supply's output is approximately +7V and is used in conjunction with post regulators on the Scan Rate Converter module to provide +5V and +3.3V. Provisions have been made for powering a tuner with the +15vs, +33vs and -12vs. The +33vs is switched on by the +12vr.

On sets supporting GemStar, a 9VS standby source is provided from +15VS via a dropping resistor to form an unregulated +12VS. This supply is fed to a switched +9V signal regulator. This regulator can be activated during RUN and Acquisition modes.

A power fail circuit with output, PWR_FAIL senses an unregulated negative supply (about -15 volts) that is proportional to the Raw B+ input. PWR_FAIL is asserted when the Raw B+ is no longer sufficient to guarantee regulation of the output voltages. The output voltages will remain in regulation for a minimum of 20 ms after PWR_FAIL is asserted.

Degaussing

Automatic Degaussing is provided via a PTC connected is series with the AC line and contacts of a relay. When the main power ZVS is activated by the on/off line, the +12v supply rises and the transistor, Q14250, driving the relay coil is saturated until the electrolytic capacitor, C14250, charges to the value determined by the base divider resistor. This differs from earlier chassis in that the opening of the relay is determined by time constant rather than uC control.

Horizontal Scan Power Supply

The scan power supply works on the same principles as the main ZVS power supply. The ZVS scan supply is driven by the main ZVS supply. The scan B+ is used to provide the error feedback signal to the ZVS scan supply. The EW pincushion, EW corner and the EW trapezoidal correction as well as the fixed width is still controlled by the TDA9151B controller. EW pin correction is achieved by modulating the Scan_B+. A low level signal is applied to the input of the scan power supply. In the flat series tubes, Scan_B+ is not modulated, but instead employs a diode modulator to achieve pincushion correction.

The ZVS scan supply is protected against overvoltage by monitoring the Scan B+ and the yoke current. If the Scan B+ rises such that the junction of R14809 and R14815 increases past the voltage drop of CR14803 (51V zener). Q14811 turns on, shutting down the gate drive of Q14800. The yoke current is monitored through a flyback pulse. The pulse is rectified by CR14807. If the rectified voltage increases enough to bias CR14805 (36V zener), Q14811 will also turn on.

The same rectified voltage at CR14807 is also used to regulate the ZVS scan supply. If the rectified voltage is not high enough to turn on Q14811, then Q14803 will turn on setting the latch controlling Q14800 gate drive.

Diode Modulator

In order to correct the inner pin associated with the flat face plate of the true flat tubes, a variation of the classic diode modulator is used. Basically the circuit is configured with S-cap C24434 as the main S-cap in the circuit at the top and bottom of the vertical raster. At the very center, the effective value of the S-cap is the series

combination of C24423 and C24418 causes the equivalent value of the S-cap to be less in the middle and therefore causes stretching of the raster gradually as the vertical scan approaches the center and then gradually decreases as it approaches the end of vertical scan. U24401 and U24401 provide gain and filtering for the WIDTH_REF line from the deflection SIP, a signal comprised of a vertical rate parabola riding on a DC level. This amplified signal drives the pin output device.

Horizontal Parabola Generator

While the horizontal circuitry is designed to operate at several frequencies, the dynamic focus Voltage wave form is required to maintain a constant peak-to-peak Voltage. For optimum performance a "bath tub" shaped waveform is required and that the wave form be phase locked to the horizontal deflection wave form. The amplitude of the low level signal is set by the Voltage divider of R24401 and R21102. U24402 is used as an error amplifier and filter. The output is a DC Voltage that is used to drive R24404. This DC Voltage is switched to ground by Q24402 at a horizontal frequency and generates a rectangular Voltage wave form. C24422 acts as a phase delay that is used to center the dynamic focus wave form. This rectangular Voltage wave form is then buffered by U24402. This buffer also provides a constant drive impedance for the double integrator, U24403.

This rectangular Voltage wave form is then AC coupled into a double integrator. The output of this amplifier is AC coupled into two different paths. The first path couples into a peak-to-peak detector. This consists of CR24403, CR24402, C24410, C24411, R24413, and R2207. The output of this detector is fed back to U24402 and compared to the reference level set by R24401 and R24402. It is by this means that the amplitude of the parabola wave form is held constant across different horizontal frequencies.

The second path AC couples the parabola wave shape into the wave shaper. This circuit is used to generate the "bath tub". It consists of C24409, R24416, R24417, R24418 and CR24401. By varying the ratio between R24416, R24417 and R24418 it is possible to control the percentage of clipping or the shape of the "bath tub" wave form. U24403 is then used as a buffer in order to drive a high Voltage amplifier.

Main Tuner

The main tuner is a single conversion, electronically aligned tuner. The main tuner of the CTC197 is used for the CTC210.

Second Tuner

The CTC197 2nd Tuner (PIP) module is used for the CTC210. The tuner is a cold version of the CTC185 tuner. It receives its signal from the RF splitter output on the main tuner.

Composite Input Switching

The Composite Video Switching supports three rear jack panel inputs, a front panel input and two composite signals from the NTSC tuners. A matrix switch, U16501, performs Composite Video switching. This arrangement will allow any Composite Video (CV) signal to be displayed as the Main or PIP Insert Picture.

The eight inputs to the CV Matrix switch are:

- Main Tuner CV
- PIP Tuner CV
- AUX-1
- AUX-2
- AUX-3
- Front CV
- Main Y
- Y from the YPrPb Input

The outputs are:

- Main CV
- PIP CV
- CV signal to the data slicer in the micro

The Closed Captioning (CC) Video output can be any of the available CV inputs or the Y from the displayed S-Video or YPrPb signal.

S-Video Input Switching:

The S-Video Switching supports three rear panel jacks, sharing the audio inputs with their respective CV inputs. The combed Y/C from the optional Frame Comb is also input to this switch. An auto detection scheme will select S-Video over CV if sync is detected on the corresponding Y/C input. The Y/C from the Comb Filter is input at the S-Video Switch in the F2PIP. This allows the Frame Comb input to be hard wired. If the control system detects the Frame Comb IC at power up it will configure the switches for Frame Comb operation. Otherwise the Comb in the F2PIP is utilized. A matrix switch, U16500, performs s-Video switching. The 8 inputs to this switch are: S-Video-1, S-Video-2, S-Video-3 and the Frame Combed Chroma and Luminance. Two pairs of Y/C outputs are selected and routed to the S-Video switch located in the F2PIP IC. This will allow the display of two S-Video sources as main and insert channel. In normal operation one Y/C input is used for the main display and the second is used to poll the other S-Video Inputs looking for sync.

F2PIP and Comb Filter

The F2PIP IC, U18100, performs both the Comb Filter and the PIP function. A three input S-Video switch is also included inside the IC. The two main inputs, Y1/C1 and Y2/C2, are fed from the S-Video Switch. The third Y/C input is from the Line Comb in F2PIP. The Video Control IC, U22300, generates a Sandcastle pulse at pin 2 from which a suitable Horizontal Drive pulse is derived. This combined with the Vertical pulse present at pin 31 provides a Composite Blanking pulse to synchronize F2PIP. The presence of sync on Y1 and Y2 can be determined over the I2C Bus and used to control the auto S-Video select. On chip A/D's, D/A's, PLL's and Memory make the F2PIP a one chip PIP solution. The F2PIP IC contains an Adaptive Comb Filter for the main picture as well as content screening and captioning for the PIP.

The Comb Filter receives Composite Video from the CV Switch. After the sync tip is clamped the signal is digitized to 8 bits. The sample clock is at 4 Fsc and phase locked to the main channel burst. The Digital comb, with two 1fH delay lines, adaptively separate the Luma and Chroma signals that are then converted back to analog. The Y/C signals are low-pass filtered externally to remove repeat spectra and routed back into the S-Video Switch in the F2PIP. Vertical peaking is provided with bus controlled gain. The CV Output and Y/C Input to the S-Video switch allow for an optional Frame Comb Module to be used to circumvent the comb filter inside F2PIP.

The Video signal to be inserted as PIP may be a Composite Video signal or a signal made by internally summing either of the two S-Video inputs. Because this is a one-clock system, the PIP signal is sampled by a clock that is locked to the burst of the main signal. If burst is not present on the main channel, F2PIP can create its own burst. Following the sampling process the composite signal is internally band-passed and low-pass filtered for Y/C separation. If the chroma carriers are similar in frequency a digital PLL allows demodulation of the PIP chroma. The PIP Y/U/V samples are stored in memory and are read out synchronized with the main picture. The PIP picture consists of 69 lines with 108 luma and 18 pairs of chroma pixels. The PIP controller also generates a Fast Switch signal that is used to control the Y/C overlay switch inside the FPIP IC. It is also used to defeat Black Stretch during time PIP is displayed.

A 1/9 size NTSC PIP can be placed almost anywhere on the main NTSC raster.

YPrPb and Digital TV interface

A three input ganged RCA jack, J22401, provides for a YPrPb or "YUV" Input. This signal is input after the chroma decoder so that the 1.0fH to 2.14fH signals can be directly processed, eliminating the chroma encoding and decoding process. The 1.0fH Y or luma signal contains standard NTSC sync. The 2.0 and 2.14 fH signals have tri-level sync and because of their line frequency require special processing. The NTSC and External YPrPb signals are switched and clamped using two CD-4053 IC's, U22402 and U22403, before being routed to the Digital Interface. The discrete clamp switch is required to allow choosing the clamping level and send it as a "Black Reference" to the DM-1 module via J22403. The VGA2_NTSC / VGA1_YPRPB control line selects NTSC or YPrPb and is shared with the VGA switch since they are mutually exclusive. The YPRPB_Y signal is routed to the CV Switch to allow decoding of Closed Caption data on the YPrPb Input.

The Y signal is routed directly to U22407, which generates the required Horizontal and Vertical Drive signals. This IC also generates a Composite Blanking signal, BLK_1300 and a Black Stretch Blanking and Clamp Key signal, SCP_1300. These two signals are used to drive the Video Control IC, U22300 for all 1.0, 2.0 and 2.14 fH signals. This allows idea control of the Blanking, Black Stretch and AKB in these modes. For NTSC operation U22407 is locked to the NTSC_H and NTSC_V signals coming from the Video Control IC, U22300. For YPrPb operation the YPRPB_H and YPRPB_V are routed to deflection.

In the CTC210 NTSC, YPrPb or the DM-1 signals are selected. J22402 provides differential YUV signals. U22404, U22405 and U22406 are configured to convert these to single YUV signals. For Digital TV applications U2204 is configured as a two input YUV switch by connecting the Matrix to ground through R22412. DIG_2H and DIG_1V are the respective Horizontal and Vertical Drive signals from the DM-1 module.

Scan Rate Conversion Process

The scan rate conversion process (also called de-interlacing or upconversion) takes an interlaced signal at 1Fh horizontal rates (15.75 KHz) and converts it to a progressively scanned picture. In order to do this, it speeds up the current line and provides an 'interpolated' line. This allows the entire frame to be scanned in one vertical sweep instead of two successive sweeps. This process creates a picture visually free of scan lines and interfield flicker.

The digital decoder takes the resulting YPrPb signal from the OSD overlay, digitizes it, and formats it into a CCIR656 data stream. For this system to work correctly, the decoder is sync master and provides horizontal and vertical signals to the Gemstar module.

The digitized video and sync signals are passed to the deinterlace IC. This IC examines the incoming video data (storing fields at a time), and determines the best way of creating the 'interpolated' lines. If there is no motion detected, the system repeats the previous field's information to provide a complete frame of non-moving video. If motion is detected, a vertical/temporal filtering is applied to the lines and fields around the interpolated line to provide a best-case line. If there is a definable, consistent reduction in motion artifacts every 5 fields in the signal, the system assumes the source was a 24Hz frame rate film signal that has been adapted to 60Hz NTSC fields via a 3:2 pull-down process, and it assembles the fields with the correct lines from previous fields. The film mode controller performs this process. The resulting 2Fh scan-rate digital video is then fed to a triple DAC for conversion to an analog signal.

NTSC Chroma Decoder and Back-end Processing

The main NTSC decoder and wide band video processing is handled by U22300 a Video/Chroma/Deflection processor IC. The U22300 processor accepts the separated luminance and chrominance signals from the comb filter. The chroma path has a **selectable peaking** circuit inside the IC. The Q and center frequency is under bus control. These are adjusted to compensate the response from the various video inputs, including RF, CV and S-Video. The luma path has a selectable 3.58 trap with delay line.

U22300 is alignment free. Because the tint function is performed at base band there is no tint-preset register available for NTSC. Following demodulation, the I/Q or U/V output signals are internally low-pass filtered and routed to the NTSC/1H_YPrPb switch. For **Auto-flesh** operation the IC must demodulate on the I/Q axis. The internal matrix can accept U/V or I/Q signals but its input follows the selection of the NTSC demodulator. With the present Matrix, the Auto-flesh will **only** operate on **1.0 fH NTSC**. In the U/V mode signals are routed around the auto-flesh circuit. Only customer presets need be aligned.

Internal to U22300 is a horizontal and vertical sync processor. The horizontal and vertical drive pulses are used to drive the deflection in the 1.0 fH mode. An internal PLL generates a stable Horizontal Drive pulse. A vertical count down scheme is used to generate a stable Vertical Drive pulse. I^2C bus registers are available to read the status of the HPLL, the field frequency and power on reset condition.

The Back-end Processor IC accepts YIQ (NTSC) or YUV video and enhances it with the following functions:

1) User controls for pix, black level, sharpness (with noise coring), color saturation, and tint.
2) Black stretch with auto-pedestal expands blacks to full dynamic range.
3) Edge replacement sharpens the luma edges.
4) SVM processing to enhance edges
5) Noise reduction to improve appearance of noisy sources
6) Auto-flesh is available, for NTSC signals only, to minimize scene to scene variations in tint
7) AKB (Automatic Kine Bias)
8) Beam current limiting

OSD for both 1H and 2H comes in following all user controls.

The **Red**, **Green** and **Blue** outputs from U22300 are clamped to prevent Blanking from going below 1.1 Volts. The Low-Pass filters remove unwanted harmonics a computer input may have. A reference voltage is provided for common mode rejection at the Kine Driver IC's. The AKB operation can be controlled over the I^2C Bus; this includes off /on and AKB Gain. With AKB off the Bias and Drive controls can be used to set color temperature. With AKB on, the bias controls set the reference input to the AKB. The AKB circuit generates Red, Green and Blue pulses at the top of the raster. The control loop moves the bias to match these currents to the reference set by the bias controls. In order for the AKB to operate U22300 must recognize the start of Vertical. The Horizontal and Vertical portions of the Blanking input, pin 25, times the AKB interval. The horizontal rate Clamp Key at pin 24 is also used in the timing generation. The AKB output pulse present at Pin 17 is used to blank the Dynamic Focus to prevent contamination.

The **SVM** low-level signal processing is also controlled by the I^2C Bus. The SVM timing, gain and parabola correction can be adjusted for different modes or conditions. The **SVM** signal is only present when the **Peaking** is activated. The **SVM** mute threshold is 0.75 Volts on the OSD Fast-switch. The OSD switching occurs at 2.25 Volts. This allows the SVM to turn off before the OSD is displayed and removes OSD before turning SVM back on. This prevents the OSD edges from being modified by the SVM.

Picture Tube Management System

The CTC210 product uses 3 Philips TDA6120Q Integrated Circuits for the Kine drivers, U15101, U15102 and U15103. The overall gain is approximately 38dB (x77) for CTC210. The CRT drivers will be used with 27", 32", 34W, 36" and 38W DV tubes. AKB & Beam Limiting is provided by the Back End Processor, U22300.

CIRCUIT OVERVIEW

A current reference for AKB is DC coupled from each IC driver. A current reference for the Automatic Beam Limiter is provided through the High Voltage Circuitry.

The RGB output section of U22300, the CRT driver circuitry, the ABL circuitry, and the AKB circuitry make up the Picture Tube Management System.

R,G,B bias controls and R(G),B drive controls are available. The R(G) control is a register that controls either the Red or the Green Drive. The Drive that is not being controlled is set to nominal. U22300 also provides an analog AKB system. The low-light color temperature is aligned by adjusting the AKB reference levels.

Afterglow prevention is provided by a grid kick circuit and a Kine driver IC cut-off circuit that operates when there is a decrease in the +12VR supply voltage.
The ABL section of U22300 and its associated circuitry will limit the average beam current through the picture tube to limit HV power.

The AKB system does compensate for Picture Tube leakage current due to the method of DC current addition and restoration.

CTC210 I/O Board Audio Circuitry

Aux. Inputs
The following audio inputs are present as jacks, that are connected electrically to the input switching circuit CMOS switches (U11400, U11401) of the Audio I/O Board. The CMOS switches are controlled by the system micro, in response to customer commands:

Stereo Audio Inputs 1, 2, 3
Three pairs of right/left audio inputs, (J16501, J16502, J16503), each pair clustered with a video input RCA-jack and one S-video jack.

Front Audio/Video Input
Allows a camcorder to be plugged in directly, via a stereo pair of RCA phono jacks. (J26104 on Front A/V board). It has stereo audio capability, and is a selectable audio input. The front A/V board interfaces to the I/O board via differential coupling (U11402) or each channel.

RCA-Jack YUV Stereo Audio
A pair of clustered input jacks (J11403) is used to input stereo audio from YUV digital video/audio source.

NTSC Stereo Audio Inputs
A pair of differential input amplifiers (U11402) are used to accept differential Left and Right NTSC audio signals from the stereo decoder from the DM1 module.

AC-3 Interface (Rt, Lt AC-3 inputs)
Differential amplifier inputs (U11404) and outputs (U11403) are provided for the CTC210.

Volume/Tone Control Function, U11800

This IC contains five main functions:
1. SELECTOR SWITCH
2. STEREO VOLUME CONTROL
3. STEREO SPEAKER FADER CONTROL
4. TONE CONTROLS
5. IIC BUS EXPANDER DIGITAL OUTPUTS
6. MUTING

SELECTOR SWITCH:
This is used to select between the following signals:
1. The selected signal being applied both to the Selected Outputs and the HI FI Outputs, as well as the signal applied to the headphones and speakers.
2. All selected NTSC input signals, coming from the input CMOS switches.

STEREO VOLUME CONTROL:
The volume control is a 1.25dB/step control with approximately 80dB of range. This linear control will be modified (in software) by a volume taper curve so that the volume OSD (on screen display) gives the desired customer "feel". This block also includes speaker fader and bass/treble controls.

SPEAKER FADER
This is utilized for a right/left balance control. It is also used for the Customer Mute function.

TONE CONTROLS
The bass/treble is used as a standard function without graphic equalizers.

IIC bus expander outputs
This pair of outputs is used to control muting of the power amplifier (Speaker Mute) and muting of the Aux. Outputs and headphone amplifier (Aux. and Headphone Mute). Outputs 1 (pin 8) and 2 (pin3), respectively.

MUTING
The main customer MUTE function is accomplished by ramping the volume control down at a rate which will not cause audible pops when a 1khz sine wave tone is present. The proper rate for this is 1 step/ms. In addition, the Speaker Volume should be ramped down at 1 or 2 steps per ms. after the main volume is ramped down.

SRS Function

The SRS® (Sound Retrieval System) function is accomplished by filtering, phase inversion, and summing circuits made with U11700 and U11701, and their associated circuitry.

The opamp stage, U11701A, buffers the left channel signal. U11701D inverts the right channel signal. The buffered left and inverted right channel signals are summed through R11723 and R11726, then filtered by the RC network consisting of R11712, C11706, R11725, and C11702. The impedance of the filter network is considerably higher than that of the summing resistors, in order to minimize component interactance. The filtered response has a midrange cut of about 10dB. The filtered stereo difference signal is then buffered by U11701B.

The left and right input signals are summed by R11714 and R11735 and form the stereo sum signal. This stereo sum signal is buffered by opamp U11701C.

The SRS difference signal filter function is switched in and out using the CMOS switch, U11702. It is controlled by transistor Q11701. At the same time, the sum signal gain is changed by saturated transistor switch Q11702 connected to CNTL_C of U11702. These switches are controlled in response to the digital "SRS_ON/OFF" signal and "SRS_FOCUS" from the micro.

When the SRS function is turned OFF, the gain and frequency response of both the sum and difference signal are flat, which renders normal stereo channels at the outputs of opamps U11700-A and B.

Compression Function

The compressor function is implemented by software control of the volume control IC U11802, in response to the dc voltage amplitude present at the output of the Compressor Detector circuit, based around opamp U11500. The dc voltage that is present at the detector output is proportional to the peak value of the audio signal. The detector output is connected to an A-to-D converter in the control micro.

Outputs

RCA-Jack Outputs
Two pairs of RCA-jacks provide two-channel stereo audio from the current program (large picture audio only, no PIP audio available). The "HIFI" output signal, J11301, is first processed by SRS, "Sound Logic" compressor, and TVB control before being passed to the output jacks. The HIFI output amplifier is also the Headphone Amplifier. The "Selected" and "NTSC Selected" output signals are routed straight through from the input switches, and are not processed.

The "Selected Outputs #1", J11300, are selected by the input switching circuit of the TVB IC, U11802, selecting the selected NTSC signals from the input switching circuit, U11400 and U11401. The "NTSC Selected" Outputs (J11302) consist only of NTSC signals from the input switching circuit, U11400 and U11401.

Power Dropout Mute Circuit

Pop-reduction (muting) of the RCA-jack output signals occurs during power on/off by grounding the inputs using bipolar transistors as analog switches. A dedicated circuit (Q11300, Q11302, Q11308 and associated circuitry) responds to both the +5V Standby and +12V run supplies. The standby supply is used to charge a large electrolytic capacitor through a diode. When power drops out the voltage on this electrolytic remains relatively constant for a significantly longer time period than the voltage on the +12V run supply. The stored charge on the +5V standby electrolytic is used to turn on muting transistors Q11901, Q11902 into saturation, this short out the Aux. Out and Headphone Amplifier signals. This muting prevents large-amplitude transient voltages from reaching the inputs to external power amplifiers.

Amplifiers

Headphone Amplifier
The Headphone Amplifier (U11900) doubles as the HIFI output amplifier. The stereo headphone jack connects to the U11900 outputs, and is located on the Front A/V panel.

The headphone-input signals are muted during power on/off by grounding the inputs using bipolar transistors as analog switches. A dedicated circuit, Q11300, Q11302, Q11308 and its associated circuitry, respond to both the +5V Standby and +12V run supplies. During momentary power outages and during normal power-up/power-down, this circuit drives the headphone amplifier input transistors Q11901, Q11902 into saturation. This muting prevents large-amplitude transient voltages from reaching the inputs to external power amplifiers or to the headphones.

PWM (Pulse-Width-Modulated) Power Amplifiers
The power amplifiers are monolithic IC's (U11901, U11902), which are "PWM" switchmode power amplifiers. Each channel provides nominal 10 watts of power into an 8 ohm loads. No heatsinks are required, as efficiency is greater than 85 %.

PWM Amplifier Operation
A triangle-wave generator operates at approx. 150 kHz. This triangle waveform is applied to one terminal of a high-speed comparator. To the other terminal is applied the analog signal to be converted to PWM. The output of the comparator is PWM. This PWM signal is applied to a push-pull output stage.

In order to realize the power-saving advantage of the PWM design, the PWM waveform must be integrated before being applied to the resistive speaker load, otherwise full power will be delivered to the load at all times, even when there is no audio input signal present. A two-pole L/C lowpass filter is set to 15khz to remove the high frequency components of the signal.

Negative feedback is picked off at the filter output and applied to the appropriate upstream node to reduce distortion and output impedance.

Mute/standby operation
Power amp muting circuitry consists of Q11906 and its associated circuitry. The muting circuit responds to control signals from the TVB IC, U11800, pin 8, which is controlled by the IIC bus.

Speaker Outputs

The stereo power amplifiers connect to either external speakers or internal speakers, depending on setting of EXTERNAL/INTERNAL DPDT speaker selector switch. This electromechanical switch is located on the rear panel of the I/O board for customer access. In the "EXTERNAL" position, the main power amplifier outputs are connected to the External Speaker jacks. In the "INTERNAL" position, the main power amplifier outputs are connected to the internal speakers.

AVR (Automatic Volume Reduction)

The AVR function is used to protect the loudspeakers from excessive power levels. A level detector circuit (Q11904 and related circuitry) provides a two-state digital signal, the state depending on the output voltage amplitude from the power amp. The digital signal is connected to one of the inputs of the system control microprocessor, where its state is polled by the system microprocessor.