CIRCUIT OVERVIEW

Caution: Hot Chassis Warning

The following circuits are considered HOT (AC line referenced) and must be serviced using an isolation transformer:

- AC Input (Main PCB)
- Horizontal Output (Main PCB)
- B+ Regulator (Main PCB)
- B+ Regulator (PTV Auxiliary PCB)

AC Line Input

The AC line is filtered (FL4001) and rectified (CR4001 - CR4004) to produce the +150V Raw B+. Raw B+ powers both the Main power supply and the PTV Auxiliary power supply.

Main Power Supply

The switch mode power supply on the Main PCB develops Regulated B+ (+143.5V), standby supplies and run supplies. Whenever AC power is supplied to the instrument, the regulator control IC (U4101) operates in the standby mode and the Regulated B+, +15V run, +7V run, +17V run, −17V run and +5V standby supplies are present. When the instrument is turned on, the system control IC (U3101) switches on the remaining run supplies (+12V, +9V, +5V and +9V Horiz. B+) and U4101 operates in the run mode.

Standby Mode

When AC power is supplied to the instrument, Raw B+ is fed to the chopper transistor Q4101 (through T4102) and to the regulator control IC U4101 (through R4003) to start the regulator circuit. U4101 turns on when the voltage at pin 16 reaches 10 volts and remains on until this voltage drops below 7.5 volts. After U4101 begins supplying drive pulses to Q4101, run voltage for U4101 is supplied by a feedback pulse from pins 12 and 13 of T4102 (rectified by CR4101).

This feedback pulse is also rectified by CR4106 and fed to the error amp inside U4101 to regulate the +5V standby supply (during standby mode, the +5V standby supply is the only supply used; the loads on the run supplies are minimal). When AC power is applied, the reference voltage (VREF) at the noninverting input of the error amp is set to 2.5 volts. U4101 sends short duty cycle, 20kHz pulses to the chopper transistor (Q4101) until the feedback voltage reaches 2.5 volts. At this time, VREF is switched to 2.25 volts, and the 20kHz drive pulses are interrupted until the feedback voltage decreases to 2.25 volts. VREF is then switched back to 2.5 volts, and the cycle continues until AC power is removed, or a turn-on command is received. Slow, controlled start-up is provided by the capacitor at U4101 pin 9. This capacitor draws current during start-up, lowering the duty cycle of the drive pulse. The internal oscillator frequency is set by R4105 and C4107.

Run Mode

When the system control IC (U3101) receives a turn-on command, pin 38 is pulled high to activate the on/off switch circuit (Q4306 on, Q4304 on, Q4301 off and Q4305 on) and supply +9 volts to the horizontal section of the one-chip (U1001 pin 26). U1001 supplies drive pulses to turn on the horizontal deflection circuit (Regulated B+ and +15V supplies for the horizontal circuit are already present). When the horizontal circuit is operational, the +26V supply from the flyback secondary turns on the +12V (Q4702), +9V (Q4704) and +5V (Q4703) run supplies to power the remainder of the Main PCB.

Regulation during the run mode is achieved by sampling the Regulated B+ (R4114, R4148, R4116 and R4115) and generating a horizontal rate PWM feedback signal (Q4105, Q4106 and Q4107), which is fed to pin 2 of U4101. A horizontal pulse from the flyback (T4401 pin 7) is used to turn Q4106 on at a horizontal rate; the "on" time of Q4106 is determined by the voltage at the collector of the error amp Q4105. If Regulated B+ decreases, Q4105 collector voltage decreases, the "on" time of Q4106 decreases and the "on" time of Q4107 decreases. This signal is inverted by T4101 so that the "on" time of the signal to U4101 pin 2 increases. In this way, the chopper transistor (Q4101) runs at horizontal rate, and the "on" time of the chopper transistor varies with the duty cycle of the feedback signal.

Switching transistor Q4109 defeats the feedback path when the instrument is turned off. This insures that no pulses from the horizontal circuit reach the regulator (causing erratic operation) after the instrument is turned off.

Overcurrent shutdown protection is provided by sampling the current through Q4101. The voltage across R4110 is divided and fed to U4101 pin 3. If this voltage exceeds the threshold level, the overcurrent shutdown logic disables the drive pulses until the voltage at pin 3 drops below the threshold.

Horizontal Deflection

Horizontal sync is derived from the luminance input to the one-chip (U1001-43 for TV Video, U1001-40 for External Video) via a sync separator internal to U1001. Horizontal deflection is locked to incoming sync by comparing the output of the sync separator with a feedback pulse from pin 7 of the flyback (AFC). The *Horizontal Phase* control (R4306) is used to shift the video signal with respect to the raster (horizontal centering).

The frequency of the horizontal VCO is determined by the crystal resonator Y4301, which resonates at 503kHz. The output of the VCO is fed to a countdown circuit, which provides a 15,734Hz drive waveform. This signal is amplified and leaves the one-chip at pin 23.

The horizontal drive signal passes through driver transistor Q4302 and is transformer-coupled (T4301) to the horizontal output device Q4401.

CIRCUIT OVERVIEW (Continued)

Power for the deflection circuits internal to U1001 is supplied by the +9V run supply, which is activated when the instrument is turned on. Power for the horizontal drive circuit (+15V supply) and the horizontal output device (Reg. B+) is available whenever the AC line is connected.

The horizontal output device switches to transfer power from the Regulated B+ supply to the secondary of the flyback (T4401). In addition to developing a feedback pulse for AFC (see above), the flyback generates high voltage for the picture tubes, a −12V supply, a +26V supply, a +200V supply, a filament pulse and a 90Vp-p pulse.

X-Ray Protection

The filament pulse from pin 5 of the flyback is rectified by CR4901 and applied to the cathode of zener CR4902 through a precision divider network. If the rectified voltage exceeds 10 volts, the zener conducts and the x-ray protect circuit at U1001 pin 22 is activated.

When active, the x-ray protect circuit disables horizontal deflection, causing the +26V flyback secondary supply to drop. Loss of the +26V supply results in loss of the +9V run supply (refer to **Main Power Supply** - Run Mode). When the +9V supply drops, the system control micro (U3101) responds by cycling the instrument off and on (refer to **System Control** - Fault Detect).

Pincushion Correction

Without correction, the raster would exhibit pincushion distortion (raster narrow at the center of the display and wide at the top and bottom of the display). The pincushion correction circuit uses a capacitor divider (C4401, C4402 and C4801) to vary the amplitude of the flyback pulse to the horizontal yoke. By controlling the discharging of C4801, the width of each horizontal line can be adjusted to eliminate distortion in the raster.

U4801 generates a horizontal rate PWM switching signal that turns Q4802 on and off. When the voltage at U4801-2 (derived from the 90Vp-p pulse at T4401 pin 7) exceeds the reference voltage at U4801-3, the output goes high, turning on Q4802. Whenever Q4802 is on, C4801 is discharged, lowering the voltage at the junction of C4401/C4402 so that more of the flyback pulse reaches the yoke (width increased). Whenever Q4802 is off, Q4801 is allowed to charge, raising the voltage at the junction of C4401/C4402 so that less of the flyback pulse reaches the yoke (width decreased).

In order to offset pincushion error, a vertical rate parabola must be added to the horizontal rate waveform at U4801-2. The vertical yoke return signal (saw + parabola) is fed to the emitter of Q4801. A vertical saw waveform is supplied to the base of Q4801 and the resulting vertical parabola at the collector is buffered (Q4803) and added to the horizontal waveform at U4801-2. The *E/W Pin Amp* control (R4805) is used to set the amount of vertical rate correction.

Width control is accomplished by adding a DC voltage to the vertical and horizontal waveforms at U4801-2. This DC voltage is adjusted with the *Width* control (R4802).

When Q4802 is turned on, energy is stored in L4803 (pins 4 and 5). When Q4802 is turned off, this energy is transferred into the +26V supply (through CR4803) and the +15V supply (through CR4806).

Switching transistor Q4804 is used to turn off the pincushion PWM (U4801) when the instrument is turned off. In this way, the ringing of the horizontal circuit (after it is turned off) does not affect the operation of the main power supply regulator as it switches to standby mode.

High Voltage Regulator

Without correction, high voltage would decrease as beam current increases. This would cause an increase in raster size that would be noticeable to the viewer, because any error on the picture tube face is magnified by the lens and mirror. To offset this effect, the high voltage regulator circuit compares a sample of high voltage to a reference voltage and provides a boost whenever high voltage starts to drop.

A sample of high voltage (approx. 60 volts) is supplied to the HV Splitter PCB from the High Voltage Splitter. This signal is impedance-matched and buffered to provide a usable HV sample to the High Voltage Regulator PCB. The sample is routed through a precision divider network to provide an error signal for the comparator (U4751). CR4751 supplies the reference voltage for the inverting input of U4751. The output of the comparator is inverted (Q4753) and applied to the B+ modulator transistors (Q4754 and Q4755). Controlling the turn-on and turn-off of these transistors controls the B+ available to the MOSFET switch Q4752.

The MOSFET switch (Q4752) is turned on during retrace by Q4751. When Q4752 is turned on, a pulse is developed across the primary of T4751. This pulse is coupled through T4751 and added to the bottom of the high voltage winding of the flyback. The amplitude of the pulse (amount of correction) is determined by the B+ voltage available to Q4752 through Q4754 and Q4755.

Vertical Deflection

The vertical reset pulse from U1001-29 turns on Q4505 to reset the vertical ramp generator Q4506. When Q4505 turns on (vertical retrace), ramp capacitors C4518 and C4519 are discharged through R4504. When Q4505 is turned off (vertical trace), C4518 and C4519 begin to charge through R4507. The supply voltage for the ramp capacitors is generated by the flyback, rectified by

CIRCUIT OVERVIEW (Continued)

CR4502, and filtered by C4504. The *Vertical Height* control (R4522) adjusts the supply voltage to the ramp capacitors to set the height of the display. R4521 and R4525 provide a feedback path to alter the charge time of C4518 so that the ramp at the collector of Q4506 is slightly nonlinear (to offset the nonlinearity of the DC feedback path from the yoke). This nonlinear vertical ramp is fed to pin 3 of the vertical drive IC (U4501).

Current for vertical deflection is provided by a horizontal rate pulse from the flyback. During horizontal retrace, T4401-2 is positive with respect to T4401-3. The current path is from T4401-2, through the vertical yoke winding, S-shaping cap C4503, current sense resistor R4505 and CR4504 to T4401-3. This path provides current to deflect the beam upward (positive current). During horizontal trace, T4401-2 is negative with respect to T4401-3. The current path is from T4401-3, through SCR501, R4505, C4503 and the vertical yoke winding to T4401-2. This path provides current to deflect the beam downward (negative current). To provide vertical deflection, the net current through the yoke is controlled by turning the SCR on and off during horizontal trace. If the SCR is off most of the time, negative current (from T4401-2 to T4401-3) cannot flow, and the net current through the yoke is positive, deflecting the beam upward. If the SCR is on most of the time, negative current (through SCR501) exceeds positive current (through CR4504), and the net current through the yoke is negative, deflecting the beam downward.

The vertical drive IC (U4501) is used to control the "on" time of SCR501. The vertical ramp (positive slope) from Q4506 is applied to the noninverting input of U4501 (pin 3). A horizontal ramp (negative slope) is applied to the inverting input of U4501 (pin 2). The horizontal ramp is obtained by rectifying (CR4501) and filtering (C4522) the horizontal pulse from T4401 pin 7. Whenever the voltage at pin 3 exceeds the voltage at pin 2 (whenever the horizontal ramp decreases below the level of the vertical ramp), the SCR is turned on, allowing current to flow from the yoke through the SCR (negative current). At the beginning of vertical scan (top of display), the vertical ramp is low and the SCR is off most of the time because the horizontal ramp drops below the vertical ramp only near the end of horizontal scan. In this case, net yoke current is positive. At the middle of vertical scan (center of display), the vertical ramp is at its midpoint and the SCR is on about half the time because the horizontal ramp drops below the vertical ramp about halfway through horizontal scan. In this case, net yoke current is zero. At the end of vertical scan (bottom of display), the vertical ramp is at its peak and the SCR is on most of the time because the horizontal ramp drops below the vertical ramp near the beginning of horizontal scan. In this case, net yoke current is negative. During vertical retrace the SCR is kept turned off to allow scan to return to the top of the display. Note that CR4504 conducts only during horizontal retrace and SCR501 conducts only during horizontal trace.

Transistor Q4507 is turned on by the system control micro (U3101 pin 36) during channel change and autoprogramming. During channel change, vertical sync is not available and the countdown circuit internal to the one-chip (U1001) reverts to its default setting. In this mode, the on-screen display moves up higher in the display. By limiting the maximum voltage at U4501-2, Q4507 forces the on-screen display back to its original position until valid sync is detected.

System Control

All system functions are controlled by the system control micro (U3101). The following is a complete list of system control inputs and outputs:

Pin 1 - Reset

When AC power is applied (instrument plugged in), +15V and +5V standby supplies are generated and fed to the system control micro. The +5V supply reaches its operating voltage first, and is fed directly to pin 19 to turn on the micro. As the +15V supply rises, CR3101 (5.6V zener) keeps the reset pin below its upper threshold (2.5V) until the +5V supply turns on the micro. When the +15V supply reaches its operating voltage, +5V is applied to the reset pin and U3101 is reset.

R3116 and CR3102 connect the 4MHz oscillator to the reset circuit so that the oscillator is defeated when the reset line drops (instrument unplugged). This conserves charge on the +5V STBY supply in order to retain memory as long as possible. Minimum memory retention time is specified at 10 seconds.

Pin 2 - Fault Detect

This input signal informs the micro of a system fault, either due to loss of the +9V run supply (XRP fault) or due to a DC fault in the audio output circuit.

If an XRP fault occurs, horizontal deflection is interrupted and the +26V secondary supply drops. This turns off the +9V run supply and pin 2 of the micro goes low. The micro responds by turning the instrument off and trying to restart (cycling off for 2 seconds, on for 1/4 second) until the fault is removed or AC power is disconnected.

If the DC voltage at either of the speaker outputs exceeds +2 volts or −2 volts, the DC detector circuit (on the Digital Audio PCB) is activated and pin 2 of the micro goes low. The micro responds by cycling the instrument off and on (see above) until the fault is removed or AC power is disconnected.

Pin 3 - IR Input

The IR remote signal is received by CR3401, then amplified and demodulated by the IR preamp (U3401). This signal is inverted by Q3401 and 5Vp-p pulses appear at pin 3 of the micro.

CIRCUIT OVERVIEW (Continued)

Pin 4 - Vert. Kill/Degauss

This pin is not used on the projection TV chassis since neither a vertical kill signal nor a degauss control signal is required.

Pin 5 - KS3
Pin 6 - KS2
Pin 7 - KS1
Pin 8 - KS0

With no customer controls pressed, these sense lines are pulled high by R3103, R3105, R3131 and R3132. When a key is pressed, a logic low from one of the scan lines appears at one of these inputs. Once a low is detected, the scan lines are toggled to identify which key is pressed.

Pin 9 - Aux 2
Pin 10 - Aux 1

These output lines are used to control the video input switch U1401. The output of U1401 (Switched Video) is selected according to the following table:

U3101-9	U3101-10	U1401-3 (Switched Video)
Logic 0	Logic 0	TV Video (from IF)
Logic 0	Logic 1	Aux 1 Video
Logic 1	Logic 0	Aux 2 Video
Logic 1	Logic 1	S-Video/"don't care"

Pins 9 and 10 are both high whenever the S-Video input is selected. When the Analog Comb (non-PIP) circuit is used, S-Video is selected by this switch. When the Analog Comb (PIP) circuit is used, S-Video is selected via Q6402,Q6403 and Q6404 on the PIP Adapter board, and logic state 1/1 becomes a "don't care" state. When the Digital Comb circuit is used, S-Video selection is performed by U6401 (on the Digital Comb PCB) under bus control; in this case, logic state 1/1 is also a "don't care" state.

Audio input selection is performed by U1600 (on the Digital Audio PCB) and is under bus control.

Pin 11 - KD1
Pin 12 - KD3/Tuning Sync

With no customer controls pressed, these drive lines are held low. When a key is pressed, one of the sense lines (pins 5 - 8) is connected to a drive line and is pulled low. Once a low is detected, the drive lines are toggled (@ approx. 200Hz) to identify which key is pressed.

If the Channel Down, Setup, Video or Audio key is pressed and held, both of the drive lines will continue to toggle after the key is decoded. If the Power, Volume Up, Volume Down or Channel Up key is pressed and held, the KD1 drive live line will continue to toggle, but the KD3 drive line will be held low after the key is decoded.

Pin 13 - Enable

This line is pulled low when device address information is being transmitted on the Data line. The Enable line is then pulled high when command data is being transmitted, then pulled low for 8μsec when data transmission is completed. Enable is logic high when inactive.

A transistor clamp (Q3303) is used to keep the Enable line low until the +5V run supply reaches its operating voltage.

Pin 14 - Data

This line contains device the address, command and status information sent to the EEPROM, the Digital Audio processor, the Digital Comb processor and the PIP processor. Data is logic high when inactive.

Pin 15 - Clock

This line synchronizes the the transfer of data between devices and is active only during data transmission. Clock is logic high when inactive.

Pin 16 - Blue OSD
Pin 17 - Green OSD
Pin 18 - Red OSD

To produce an on-screen display character, one or more of the OSD outputs is pulled high at the appropriate time. The OSD outputs are logic low when inactive.

Pin 19 - VDD
Pin 20 - VSS

The system control microprocessor is powered from the +5V STBY (standby) supply; pin 20 is the ground return.

Pin 21 - Blanking

This line goes low to produce the black border around the OSD characters. Blanking is logic high when inactive.

Pin 22 - System Reset

This line is used to reset the Digital Audio processor, the Digital Comb processor and the PIP processor when the instrument is turned on.

During standby mode, System Reset is held low. When the instrument is turned on, pin 22 is pulled high after a one second delay to reset the peripheral processors, after which time system communications may begin.

Pin 23 - H Sync
Pin 24 - V Sync
Pin 25 - R1
Pin 26 - VCO

The inputs at pins 23 and 24 provide horizontal and

CIRCUIT OVERVIEW (Continued)

vertical timing for the OSD signals (pins 16, 17 and 18). Pins 25 and 26 are external control pins for the phase-locked loop.

Pin 27 - Speakers Off

This line is pulled high to mute the internal (TV) speakers during instrument turn-on and turn-off. Pin 27 is also activated via the Audio menu to turn off the internal speakers.

Pin 28 - Mono/RF Switch

This line is used to select the tuner RF input (Antenna A or Antenna B). A logic low selects Antenna A; a logic high selects Antenna B.

Pin 29 - TV Pix

This line is used to select the appropriate amplification and filtering of luminance and chrominance signals (internal to U1001) by shifting the DC voltage at pin 31 of U1001.

When the video from the IF (TV Video) is selected, pin 29 goes high and the DC level at U1001-31 increases to approx. 4.5 volts. A logic circuit internal to U1001 responds by routing the chroma signal through a narrow BPF and selecting the luma signal at pin 43 (2Vp-p luma).

When an external video signal (Aux 1, Aux 2 or S-Video) is selected, pin 29 goes low and the DC level at U1001-31 decreases to approx. 1.5 volts. A logic circuit internal to U1001 responds by routing the chroma signal through a wideband filter and selecting the luma signal at pin 40 (1Vp-p luma).

Pin 29 is also used in instruments *without* Pix-In-Pix (CTC169BL,BN) to defeat the IF circuit when an external video input is being viewed. When an external video input is selected, pin 7 (IF AGC) of U1001 is pulled low. This prevents TV Video information from contaminating the external video signal.

Pin 30 - Volume/SRS/Graphic EQ

This output is not used on CTC169 projection TV.

Pin 31 - Tint
Pin 32 - Color
Pin 33 - Contrast
Pin 34 - Brightness
Pin 35 - Sharpness

Pins 31 through 35 are PWM (pulse width modulated) outputs that are filtered to produce variable DC control voltages for picture control. The *Sub-Brightness* control (R3346) is used to compensate for production tolerances by adjusting the range of the brightness control.

Pin 36 - Channel Change

This line goes high during channel change and during autoprogramming, killing the video input to U1001 (forcing the horizontal oscillator to free-run) and clamping the horizontal ramp input to the vertical drive IC (U4501). This is done to maintain a stable OSD display during channel change and autoprogramming (refer to **Vertical Deflection**).

Pin 37 - AFT

This input is used to detect AFT crossover during the tuning algorithm. The voltage at pin 37 can vary between 0 and 5 volts, and crossover occurs at 2.5 volts.

Pin 38 - TV On

This line is held low during standby. When a turn-on command is received, this line is pulled high to start the horizontal deflection circuit.

Pin 39 - 4MHz Oscillator Out
Pin 40 - 4MHz Oscillator In

A 5Vp-p 4MHz signal is present whenever AC power is applied. Pin 39 should be used for monitoring the oscillator.

Tuner (MTP-M-2030)

The MTP-M-2030 tuner includes three antenna connections (ANT A, ANT B and CONVERTER OUT) which are selected via the SETUP menu and controlled by the system control micro (U3101). When ANT A is selected, U3101 pin 28 is pulled low. This pulls pin 10 of the tuner low, and the signal at the ANT A input is fed to the RF tuning section of the tuner. At the same time, the signal at the ANT B input is routed to the CONVERTER OUT connector. When ANT B is selected, U3101 pin 28 (and pin 10 of the tuner) goes high, and the signal at the ANT B input is fed to the RF tuning section of the tuner.

Frequency synthesis and band switching circuits are contained within the tuner. Tuning commands are generated by the system control micro; data and clock signals appear at pins 7 and 8 of the tuner. The RF AGC signal enters the tuner at pin 1, and the IF output leaves the tuner at pin 3.

Video IF

The 4.5MHz IF signal from pin 3 of the tuner is amplified (Q2301), filtered (SF2301) and applied to the differential input of the one-chip (U1001 pins 9 and 10). U1001 generates baseband video (pin 45), AFT (pin 50) and AGC (pin 2) signals. The AFT signal is sent to the system control IC (U3101 pin 37) to control fine tuning of the incoming RF signal. The AGC signal is sent to the tuner (pin 1) to optimize the gain of the RF amplifier stages.

The baseband video signal is buffered (Q2302) and 4.5MHz FM audio information is removed (CF2301). The video signal (referred to as TV Video) is buffered by Q2701 and sent to video switch U1401 (all models) and the PIP module (CTC169BM,BP only).

CIRCUIT OVERVIEW (Continued)

Audio IF

The baseband video signal at U1001 pin 45 also contains 4.5MHz FM audio information. The baseband signal is passed through a 4.5MHz filter (CF1201) and the resulting FM audio signal is fed back to U1001 at pin 51. The signal is limited and detected by U1001 and wideband audio (WBA) appears at pin 52. Baseband audio is buffered by Q1201 and the *Wide Band Audio* control (R1204) is adjusted for the proper signal level at the input of the Digital Audio circuit.

Luminance Processing

The luminance signal from either JS6400-7 of the Digital Comb board (CTC169BL,BP), JS6400-7 of the PIP Adapter board (CTC169BM) or U2601-7 (CTC169BN) is fed to pins 40 and 43 of the one-chip (U1001). Due to the design of the IC (the IC was designed to be capable of providing 2X gain for an external video signal), both a 2Vp-p signal and a 1Vp-p signal must be provided to the IC. The 2Vp-p signal appears at pin 43 and Q2707 provides a 1Vp-p signal at pin 40. During channel change and during autoprogramming, pin 29 of U3101 (TV Pix) pulls the TV Video input (U1001-43) high to prevent video from reaching the sync separator (see **System Control**).

Contrast Control

The luminance signal is fed to an amplifier whose gain is controlled by a DC voltage generated by the system control IC (contrast control). This DC voltage determines the peak-to-peak amplitude of the luminance signal at pin 38. This control voltage also affects the gain of the chrominance input amplifier at pin 31 (color tracking).

To prevent picture blooming on extremely bright scenes (high average beam current), a beam limiter circuit (Q2703) pulls down the contrast control voltage (and the brightness control voltage) to reduce beam current.

To prevent picture distortion due to high white peaks in the luminance signal, a peak limiter circuit (Q2704 and Q2705) pulls down the contrast control voltage to limit the peaks.

Sharpness Control

The luminance signal from pin 38 passes through delay line DL2701 to compensate for chroma pocessing delays. The *Contrast Preset* control (R2730) is used to set the amplitude of the luminance signal at the color driver transistors (Q2903, Q2904 and Q2905).

The signal is then buffered and filtered to separate the high-frequency and low-frequency components. Low-frequency luminance returns to U1001 at pin 35. High-frequency luminance returns to U1001 at pin 34, along with a DC control voltage generated by the system control sharpness PWM (U3101 pin 35). This DC voltage controls the gain of the high-frequency luminance amplifier (internal to U1011) to adjust the amount of high frequency information in the luminance signal. The amplitude-adjusted high-frequency luminance signal and the low-frequency luminance signal are added and fed to the brightness control circuit.

Brightness Control

The luminance signal is then fed to the brightness control circuit, where a DC control voltage (generated by the system control brightness PWM at U3101 pin 34) is used to shift the DC level of the luminance with respect to blanking. The resulting signal is buffered (Q2911 and Q2906) and fed to the R/G/B Drive circuit.

Chrominance Processing

The chrominance signal from either JS6400-8 of the Digital Comb board (CTC169BL,BP), JS6400-8 of the PIP Adapter board (CTC169BM) or U2601-6 (CTC169BN) enters the one-chip at pin 31 and passes through the first chroma amp to a pair of bandpass filters. A narrow BPF is used when the source of the chrominance signal is video from the IF circuit. A wideband filter is used when the source of the chominance signal is video from an external input (Aux 1, Aux 2 or S-Video). The DC voltage at pin 31 controls a switch which selects the properly filtered chrominance signal. This DC voltage is driven by the system control TV Pix line from U3101 pin 29 (see **System Control**).

The selected signal is routed through the second chroma amp to the color demodulator, which produces R−Y, G−Y and B−Y signals at pins 15, 17 and 18. The gain of the second chroma amp is controlled by both the color control voltage (generated by the system control color PWM at U3101 pin 32) and the contrast control voltage from U1001 pin 41.

The selected signal is also routed through a burst-keyed amp whose output is used to control the gain of the first chroma amp (ACC - Automatic Color Control) and the color killer circuit. The color killer circuit pulls down the color control DC voltage if incoming burst is too weak to produce a viewable picture.

The DC control voltage at pin 44 adjusts the hue (tint) of the demodulated color signal. The control voltage is generated by the system control tint PWM at U3101 pin 31. The *Tint Preset* control (R2816) is used to preset the tint control voltage when the customer tint control (Video menu) is at midrange.

The *Chroma Filter* control (R2802) is used to adjust the 3.58MHz oscillator and the chroma bandpass filters. The 3.58MHz oscillator can be accurately measured by forcing pin 44 to approx. 1.3VDC and measuring the frequency at the B−Y output (pin 18).

R/G/B Drivers

The R−Y, G−Y, B−Y and buffered −Y signals are fed to driver transistors Q2903, Q2904 and Q2905 to produce R, G and B signals. On-screen display information is added to the R/G/B signals via Q2908, Q2909 and Q2910.

The R/G/B signals are sent to the PTV Auxiliary PCB where they are routed to the three Kine Driver circuit boards.

Each color signal enters a Kine Driver board at pin 7 of J5001 (R, G or B). It is applied to the emitter of common base amplifier Q5001 to produce the voltage

CIRCUIT OVERVIEW (Continued)

waveform that drives the picture tube. Switching transistors Q5002 and Q5003 are a part of the scan loss protection circuit (refer to **Scan Loss Protection**). The focus and screen voltages for all three tubes are supplied from the Focus/Screen assembly. The anode voltages for the three tubes supplied from the High Voltage Splitter assembly.

Video Input/Output Circuit

In addition to the video signal from the tuner (TV VIDEO), the CTC169PTV chassis is equipped to accept the following video inputs:

Auxiliary Video Input 1 (AUX 1)
Auxiliary Video Input 2 (AUX 2)
S-Video Input (S-LUMA and S-CHROMA)

This chassis is also equipped to provide the following video outputs:

Selected Video Output (SELECTED VIDEO)

Analog Comb, Non-PIP Instruments (CTC169BN)

The function of the Video Input/Output circuit is to provide S-CHROMA and SWITCHED VIDEO signals directly to the signal processing circuit. SWITCHED VIDEO can be either TV VIDEO, AUX VIDEO 1, AUX VIDEO 2 or S-LUMA (selected by U1401) and is sent to the analog comb filter to provide luminance and chrominance signals to the one-chip U1001 (S-CHROMA is fed directly to the one-chip via Q1404 and Q1405, which are switched by U1401). The SWITCHED VIDEO signal also appears at the SELECTED VIDEO output.

Analog Comb, PIP Instruments (CTC169BM)

The switching circuits for selecting the desired video signals are distributed among several circuit areas. The function of the Video Input/Output circuit is to provide S-LUMA, S-CHROMA and SWITCHED VIDEO signals to the PIP Adapter board and the PIP module. SWITCHED VIDEO can be either TV VIDEO, AUX 1 VIDEO or AUX 2 VIDEO; this signal, along with a second TV VIDEO signal is sent to the PIP module, which selects the SELECTED VIDEO signal and the PIP VIDEO signal (small pix). Note that this arrangement allows the TV VIDEO signal to be viewed as both the big pix and small pix; this is useful when aligning the PIP module to match the color temperature of the small pix to the big pix.

The SELECTED VIDEO signal is sent to the SELECTED VIDEO output jack and to the analog comb filter (U2601), which separates the video signal into the luma and chroma components (MAIN VIDEO) necessary for the PIP module to create a pix-in-pix display. At this point, customer selection may allow the S-VIDEO signals (S-LUMA and S-CHROMA) to be sent back to the PIP module instead of the combed luma and chroma signals. This allows the S-VIDEO input to be viewed as the big pix (MAIN VIDEO). Note that the S-VIDEO signals cannot be directly used for the small pix; in order to view the S-VIDEO signal in the small pix, a normal video output from the S-VIDEO source must be connected to the AUX 1 input.

The PIP module then combines the selected signals and sends luminance and chrominance signals (containing MAIN VIDEO + PIP VIDEO) to the one-chip (U1001). Refer to **Pix-In-Pix Circuit** for details.

Digital Comb, Non-PIP Instruments (CTC169BL)

The switching circuits for selecting the desired video signals are distributed among several circuit areas. The function of the Video Input/Output circuit is to provide S-LUMA, S-CHROMA and SWITCHED VIDEO signals to the Digital Comb board. The S-VIDEO signals are sent directly to the Comb Filter board. SWITCHED VIDEO can be either TV VIDEO, AUX VIDEO 1 or AUX VIDEO 2 (selected by U1401); this signal is sent to the Digital Comb board and also appears at the SELECTED VIDEO output jack. The Digital Comb board selects the picture to be displayed on the screen (SWITCHED VIDEO or S-VIDEO) and provides luminance and chrominance signals to the one-chip (U1001). Refer to **Digital Comb Circuits** and **Pix-In-Pix Circuit** for details.

Digital Comb, PIP Instruments (CTC169BP)

The switching circuits for selecting the desired video signals are distributed among several circuit areas. The function of the Video Input/Output circuit is to provide S-LUMA, S-CHROMA and SWITCHED VIDEO signals to the Pix-In-Pix module and the Digital Comb board. The S-LUMA and S-CHROMA signals are fed directly to the Digital Comb board. SWITCHED VIDEO can be either TV VIDEO, AUX VIDEO 1 or AUX VIDEO 2 (selected by U1401); this signal, along with a second TV VIDEO signal is sent to the PIP module, which selects the SELECTED VIDEO signal and the PIP VIDEO signal (small pix). Note that this arrangement allows the TV VIDEO signal to be viewed as both the big pix and small pix; this is useful when aligning the PIP module to match the color temperature of the small pix to the big pix.

The SELECTED VIDEO signal is sent to the SELECTED VIDEO output jack and to the digital comb IC (U6401), which separates the video signal into the luma and chroma components (MAIN VIDEO) necessary for the PIP module to create a pix-in-pix display. At this point, customer selection may allow the S-VIDEO signals (S-LUMA and S-CHROMA) to be sent back to the PIP module instead of the combed luma and chroma signals; this allows the S-VIDEO input to be viewed as the big pix (MAIN VIDEO). Note that the S-VIDEO signals cannot be directly used for the small pix; in order to view the S-VIDEO signal in the small pix, a normal video output from the S-VIDEO source must be connected to the AUX 1 input.

The PIP module then combines the selected signals and sends luminance and chrominance signals (containing MAIN VIDEO + PIP VIDEO) to the one-chip (U1001). Refer to **Digital Comb Circuits** and **Pix-In-Pix Circuit** for details.

CIRCUIT OVERVIEW (Continued)

Digital Comb Circuits

In addition to the digital comb filter circuit, the Digital Comb PCB contains white stretch, black stretch, S-video switching and pix-in-pix (PIP) interface circuits. The following descriptions cover the CTC169BL chassis (non-PIP). Differences between the CTC169BL and CTC169BP (PIP) chassis' are covered at the end of this section.

Digital Comb Filter

The SWITCHED VIDEO signal from U1401 enters the Digital Comb board at JS6400 pin 1. The signal is buffered (Q6403), filtered (L6403, C6412) to prevent aliasing, and fed to pin 29 of the Digital Comb IC (U6401). The video signal is digitized and combed to produce separate luminance and chrominance signals. The luma and chroma signals are converted from digital to analog and appear at pins 33 and 9, respectively.

S-Video Switching

The digital comb IC (U6401) has provisions to switch between the combed luma/chroma signals and external luma/chroma signals from the S-Video input. The combed signals reenter the IC at pins 35 and 7; the S-LUMA and S-CHROMA signals enter the IC at pins 39 and 3. Switching is performed inside U6401 on instructions from the system control micro (U3101); the selected signals appear at pins 31 and 11. The chroma signal is buffered (Q6402, Q6414) and sent to the Main PCB via JS6400 pin 8. The luma signal is processed by the white stretch and black stretch circuits, then sent to the Main PCB via JS6400 pin 7.

White Stretch

The purpose of the white stretch circuit is to enhance the contrast of low brightness scenes. Whenever the average picture level (APL) is below 30IRE, the gain curve of the circuit is nonlinear. For signal levels below 50IRE, the slope of the gain curve is greater than one (0IRE in yields 0IRE out, 50IRE in yields 62IRE out). For signal levels above 50IRE, the slope of the gain curve is less than one (50IRE in yields 62IRE out, 100 IRE in yields 100 IRE out). Whenever the APL is greater then 30 IRE, the gain curve of the circuit is linear (no stretch occurs).

The nonlinear gain characteristic is accomplished by creating two signal paths (Q6404 and Q6405) and controlling how these two signals are mixed. When the signal level is less than 50IRE, both Q6404 and Q6405 are conducting and no current flows through R6438. The signals from Q6404 and Q6405 pass through QQ6407 and Q6408, and are mixed by Q6406, Q6409, Q6410 and Q6411. When the signal level is greater than 50IRE, Q6405 is turned off and Q6404 provides a signal to both Q6407 and Q6408. These signals are mixed in the same manner (as signals below 50IRE), but the overall gain of the circuit is changed to affect the slope of the gain curve. The resultant luminance signal is buffered (Q6412) and fed to the black stretch circuit.

Black Stretch

The purpose of the black stretch circuit is to enhance the contrast of high brightness scenes. Whenever the average picture level (APL) is high, the gain curve of the circuit is nonlinear. For signal levels below 50IRE, the slope of the gain curve is greater than one (12IRE in yields 0IRE out, 50IRE in yields 50IRE out). For signal levels above 50IRE, the slope of the gain curve is one (50IRE in yields 50IRE out, 100 IRE in yields 100 IRE out). In this manner, the dark portions of a high brightness scene are driven farther into black (in some cases, below 0IRE). Whenever the APL is low, the gain curve of the circuit is linear (no stretch occurs).

Black stretch is performed by U6402, and the enhanced signal appears at pin 5. Due to the fact that some portions of the signal are driven below 0IRE, a sync correction circuit (Q6423, Q6427, Q6428 and R6488) is used to pull the sync portion of the luma signal down to −80IRE. The luminance signal is then buffered (Q6424) and sent to the Main PCB via JS6400 pin 7.

Non-PIP Signal Flow

SWITCHED VIDEO (TV VIDEO, AUX1 VIDEO or AUX2 VIDEO) from U1401 is sent to the digital comb IC via JS6400 pin 1. The Digital Comb IC selects (via system control commands) which signal (SWITCHED VIDEO or S-VIDEO) to be used for the main picture (MAIN VIDEO). MAIN VIDEO (as luma and chroma signals) is sent back to the Main PCB to be processed by the one-chip and displayed on the screen. The SWITCHED VIDEO signal is sent to the Selected Video output (SELECTED VIDEO) via R1434 in the Video In/Out circuit of the Main board.

PIP Signal Flow

Several jumpers are added to or deleted from the Digital Comb board to accomodate the Pix-In-Pix module. All signals used by or generated by the PIP module pass through the Digital Comb board.

SWITCHED VIDEO (TV VIDEO, AUX1 VIDEO or AUX2 VIDEO) from U1401 is sent to the PIP module, along with a separate TV VIDEO line. The PIP module selects (via system control commands) which signal (SWITCHED VIDEO or TV VIDEO) to be used for the Selected Video Output (SELECTED VIDEO) and the small picture (PIP VIDEO). SELECTED VIDEO is sent to the Digital Comb board to be processed; at this point, the Digital Comb IC selects (via system control commands) which signal (SELECTED VIDEO or S-VIDEO) to be used for the main picture (MAIN VIDEO). MAIN VIDEO (as luma and chroma signals) is sent back to the PIP module and mixed with PIP

Continued

VIDEO to create luma and chroma signals for the display.

Pix-In-Pix Circuit

The SPIP module produces SELECTED VIDEO and PIP VIDEO signals and, via the fast switch IC (U8205), mixes PIP VIDEO with the MAIN VIDEO signal (from either the Digital Comb board or the analog comb circuit) for viewing. The MAIN VIDEO Y/C signals pass through the module relatively unaffected, while the PIP VIDEO signal is derived from digitizing the small pix video source. The module selects either the MAIN VIDEO Y/C signals or the digitized Y/C signals from the PIP processor (MAIN VIDEO + PIP VIDEO) to produce the picture on the screen.

Input Selection and Y/C Separation

This stage selects the desired video source to fill the big and small pix areas of the screen. The TV VIDEO and SWITCHED VIDEO inputs are composite video signals and must be separated into component luminance and chrominance signals. The SELECTED VIDEO (big pix) Y/C separation is performed by the digital comb IC on the Digital Comb board (or the analog comb IC on the Main board) and returns as MAIN VIDEO, while the PIP VIDEO signal is separated into Y and C components within the SPIP module.

Y/C to R−Y/B−Y Decoder

The insert (PIP VIDEO) luma and chroma signals enter the decoder stage (U8301) for conversion into R−Y and B−Y color difference signals, which are applied to the PIP Processor U8501. Composite sync is separated from the luminance signal and is applied to the H/V processor (U8503). Note that the PIP VIDEO luminance (Y) signal is applied directly to the PIP Processor.

3.58 MHz Oscillator - U8401

The 3.58 MHz oscillator provides a continuous 3.58 MHz signal to the encoder stage and to the PIP processor. The oscillator is locked to the color burst of the big pix (MAIN VIDEO) chroma signal. The encoder chip (U8402) uses the signal to produce the 3.58 MHz chroma signal for the output stage.

H/V Sync Signals

The horizontal and vertical sync outputs of the H/V processor stage are locked to the composite sync output of the decoder stage. The H/V processor free runs in the absence of composite sync to maintain H and V pulses to the PIP processor. These sync signals are used by the PIP processor to time the writing of insert pix video information to the VRAM.

Horizontal and vertical sync pulses from the deflection circuit (Main board) are also applied to the PIP Processor. The PIP processor contains a voltage-controlled 20MHz oscillator to synchronize its internal timing with external horizontal sync signals. When the small pix is turned on, horizontal sync from the chassis deflection circuit is compared to an internally generated phase reference to produce the error voltage for the VCO.

The horizontal blanking and vertical reset signals from deflection are also used by the PIP processor as timing signals to read small pix information from the VRAM.

PIP Processor (U8501)

The A/D converter within the PIP processor converts the analog Y, B−Y, and R−Y signals into digital information. The big pix (MAIN VIDEO) chroma signal is used as a reference to establish the chroma level for the small pix.

The digital processing stage receives the digital video information from the A/D converter and stores two fields of video into the VRAM U8502. Once in RAM, the digital data can be recalled and manipulated by the digital processing stage.

The control stage receives commands from the control micro U8901 through the three wire serial communications bus (PIP Clock, PIP Data, and PIP Enable). The control stage manages the functions of the digital processing stage to produce the various PIP features and functions. The initial PIP commands come from the system control micro U3101 on the Main circuit board.

The manipulated digital data from the digital processing stage enters the D/A converter to produce the analog Y, R-Y and B-Y signals that are fed to the output stages of the SPIP module. These signals contain the information for the small pix (PIP VIDEO). During full field effects such as freeze or zoom, these signals are used to produce the picture on the entire screen.

R−Y, B−Y to Y/C Encoder (U8402)

The encoder chip (U8402) receives the Y, R−Y, B−Y, and G−Y (derived from R−Y and B−Y) signals from the PIP processor and produces a 3.58 MHz PIP chroma signal and a PIP luminance signal containing composite sync. The 3.58 MHz signal used for the R, G, B-Y to chroma conversion is the inverted FXTAL signal from U8401.

Fast Switch (U8205) and Output

The fast switch IC (U8208) takes the PIP VIDEO Y/C signals from the encoder and mixes them (by switching) into the big pix (MAIN VIDEO) Y/C signals to create the video signal that is viewed on the screen. The fast switch control line inserts (switches) each line of the small pix video into the appropriate line of the big pix video.

CIRCUIT OVERVIEW (Continued)

The fast switch is also responsible for clamping the back porch blanking level of the small pix luma signal to the blanking level of the big pix. The Y/C output of the fast switch is applied to the Y and C inputs of the one chip to produce the big and small pix images on the screen.

Stereo Audio Circuit

In addition to the wideband audio signal from the tuner (WBA), the CTC169PTV chassis is equipped to accept the following audio inputs:

- Auxiliary Audio Input 1 (used in conjunction with the AUX VIDEO 1 input and the S-VIDEO input)
- Auxiliary Audio Input 2 (used in conjunction with the AUX VIDEO 2 input)

This chassis is also equipped to provide the following audio outputs:

- Selected Audio Output (fixed line level)
- Hi-Fi Audio Output (volume-controlled)
- External Speaker Output

The operating range of the Digital Stereo Processor (U1600) is 0 volts (ground) to 5 volts (B+). Because of this, the WBA (wideband audio) and AUX (auxiliary input) signals are biased up to +2.5 volts at the inputs to the processor. The bias voltage is generated internally by the processor and appears at pin 14. The processor performs all stereo demodulation, signal selection and volume control functions; it receives instructions from the system control IC (U3101) via the DATA line.

The SELECTED AUDIO signals are fed directly to the Selected Audio Output jacks on the rear panel. The HI-FI AUDIO signals are buffered (Q1413 and Q1414) and appear at the Hi-Fi Audio Output jacks on the rear panel.

The HI-FI AUDIO signals are also fed to a pair of 10 watt amplifiers (U1901 and U1902) to drive both the internal speakers and the external speakers. Selection of Internal or External speakers is performed by a switch on the rear panel.

A fault detect circuit is employed to prevent speaker and power amp damage due to excessive DC voltage. If the DC voltage at the Right speaker output goes positive, Q1903 turns on, lowering the voltage at the base of Q1902. This turns on Q1902, which raises the voltage at the base of Q1907. When Q1907 turns on, the system control micro responds by cycling the instrument off and on (refer to **System Control** - Fault Detect). If the DC voltage at the Right speaker output goes negative, Q1904 turns on, raising the voltage at the base of Q1907. When Q1907 turns on, the system control micro responds by cycling the instrument off and on (refer to **System Control** - Fault Detect). In the same manner, Q1905 and Q1906 provide protection from excessive DC voltage at the Left speaker output.

A muting circuit (Q1110 - Q1115) is provided to pull both the SELECTED AUDIO and HI-FI AUDIO lines low during instrument turn-on and turn-off. This eliminates any transients on the audio lines when the instrument is turned on or off. In addition, the power amplifiers (U1901 and U1902) are disabled via Q1901 (SPEAKER OFF line) during instrument turn-on and turn-off. The SPEAKER OFF line can also be used to turn off the internal and external speakers so that the SELECTED AUDIO OUT signal can be used alone.

Low Level Attenuator

In some instruments, an attenuator circuit is used to reduce low-level noise. The attenuator circuit (Q1601, Q1102 and Q1103) reduces the signal level at the HI-FI AUDIO outputs when volume is set below midrange. When volume is set to midrange or above, the system control micro instructs the digital audio processor to generate a 315kHz square wave at pin 4 (LOOP OUT). This signal is filtered to produce a DC voltage which turns on Q1601. This turns off Q1102 and Q1103, allowing the HI-FI AUDIO signals to pass unattenuated. At low volume levels, the 315kHz square wave is disabled, Q1601 turns off, Q1102 and Q1103 turn on and the HI-FI AUDIO signals are attenuated.

Dynamic Noise Reduction (DNR)

In some instruments, a dynamic noise reduction circuit is used to reduce low level noise. This circuit consists of a pair of gain-controlled filters which are used to reduce high frequency noise when signal level is low. The circuit monitors signal level at the Left and Right Selected Audio lines; when signal level is high, no filtering occurs. When signal level drops, the DNR circuit filters the Left and Right HiFi Audio lines to reduce background noise.

PTV Auxiliary Power Supply

A separate switching power supply is used to provide +15V, −15V, +45V and −45V supplies for the convergence circuits. The auxiliary power supplies are regulated by U7004 and power for these supplies is derived from the +150V Raw B+.

To prevent damage to the IC during start-up, Raw B+ is resistively dropped and clamped to 24 volts by R7136 and CR7074. When the instrument is turned on, horizontal pulses from the filament winding of the flyback (T4401 pin 5) pass through T7002 to cross the hot-cold barrier. The secondary pulses are rectified by CR7075, R7189 and C7102, and the resulting DC voltage turns on Q7050 and Q7051, supplying power to the IC. After the regulator starts, run voltage (approx. +15.5V) is supplied through CR7064.

The filament pulse is also applied to pin 4 of U7004 to lock the oscillator to horizontal rate. The IC produces 15Vp-p PWM (pulse width modulated) pulses which turn the output transistor (Q7037) on and off. Q7037 collector pulses are coupled through T7100 to four secondary windings and a feedback winding. Pulses at the four secondary windings are rectified to produce the +15V, −15V, +45V and −45V supplies.

CIRCUIT OVERVIEW (Continued)

Pulses from the feedback winding (T7100 pin 3) are rectified by CR7073 and C7077 and applied to the error amp inverting input (pin 2) through the *B+ Adjust* pot. The error amp produces an error signal whenever the inverting input deviates from 1/2VREF (2.5VDC). The *B+ Adjust* is adjusted for correct supply voltage at the +15V source.

Current through the output transistor (Q7037) is sampled by R7132 and a voltage representing the current is fed to pin 3 of the IC. Turn-on time of the PWM generator is synced to horizontal by the filament pulse (see above) and turn-off time occurs when the voltage at pin 3 equals the voltage produced by the error amp.

If the secondary supplies drop (load variation), the supplies draw more energy from T7100 and less energy is available to the feedback winding. The voltage at pin 2 decreases, the error voltage increases and the output transistor must remain on longer for the current sense voltage to reach the error voltage. If Raw B+ drops (line variation), the slope of the current sense waveform decreases and again the output transistor must remain on longer for the current sense voltage to reach the error voltage.

A slow-start circuit is used to allow the regulator to start properly. CR7058 and C7085 prevent the output of the error amp (pin 1) from going high and staying high until feedback pulses are generated. Instead, the error voltage (and the +5V reference voltage at pin 8) is used to charge C7065 to +5 volts. This keeps the width of the PWM output pulse narrow until feedback pulses are developed.

Scan Loss Protection

The PTV picture tubes are very easily damaged if horizontal or vertical scan is lost and beam current is concentrated on a small area of the phosphor. To prevent such damage, a circuit is included which monitors both horizontal and vertical scan, and cuts off the picture tubes if either is lost. This circuit operates not only in the event of a fault, but also operates during instrument turn-on and turn-off.

Horizontal Scan Detect

Horizontal scan is monitored by looking at the filament pulse from the flyback (T4401 pin 5). During normal operation, the peak voltage of the filament pulse is greater than the +10V reference. This turns on Q7043 and the pulse at Q7043-C is integrated and applied to the non-inverting input of the comparator (U7005 pin 3). During normal operation, the integrated voltage exceeds the reference voltage at the inverting input of the comparator (U7005 pin 3) and the comparator output is high (+15V). The purpose of Q7043 is to check the amplitude of the filament pulses and the purpose of the integrator (R7168 and C7091) is to check the frequency of the filament pulses. A high output at U7005 pin 1 turns on Q7044, which turns on Q7042 (assuming that vertical scan is present, causing the emitter of Q7042 to be high) and Q7048. During horizontal scan loss, the voltage at U7005 pin 3 floats low, the comparator output drops to ground, Q7044 and Q7042 turn off and Q7048 turns off, allowing its collector to go high.

Vertical Scan Detect

Vertical scan is monitored by looking at the voltage on the vertical "S" cap (C4503). This vertical signal is AC-coupled via C7105 and added to the +10V reference (CR7080) using Schottky diodes (because of their low forward voltage). As long as vertical scan is present, the voltage at the non-inverting input of the comparator (U7005 pin 5) exceeds the reference voltage at the inverting input (pin 6) and pin 7 is high (+15V). A high output at U7005 pin 7 turns on Q7042 (assuming that horizontal scan is present, causing the base of Q7042 to be low) and Q7048. During vertical scan loss, the voltage at U7005 pin 5 floats low, the comparator output drops to ground, Q7042 turns off and Q7048 turns off, allowing its collector to go high.

Scan Loss Operation

During normal operation, the collector of Q7048 is pulled low. This keeps Q5002 and Q5003 (located on the individual Kine Driver boards) turned off and the picture tubes operate normally. If either (or both) horizontal or vertical scan is lost, Q7048 is turned off (see above) and its collector is pulled high through CR5001 and R5005. Both Q5002 and Q5003 are turned on to reduce beam current; Q5002 turns off the video driver (Q5001) and Q5003 drives the G1 grid negative. CR5005 is used to prevent the G1 grid from rising too quickly when the scan resumes.

Dynamic Focus

The Focus grid of a picture tube is used to optimize the spot profile (size and shape) of the electron beam that strikes the phosphor. As the beam travels from the center of the screen to a corner, the spot profile changes, and the voltage required to focus the beam changes. The dynamic focus circuit modulates the focus voltage to keep spot size and shape more consistent.

The modulating waveform has two components: 1) a horizontal-rate parabola and 2) a vertical-rate parabola. The horizontal-rate parabola is obtained by integrating the horizontal yoke current (T7001 and C7080) and the vertical-rate parabola is generated on the Convergence PCB. The two waveforms are combined at Q7040 and sent directly to the Focus/Screen assembly.

Convergence Signal Generator

Since each color (red, green and blue) has a dedicated picture tube, convergence circuits are required to make the three rasters the same size and shape and align them on top of each other. The Convergence board includes circuits which generate various correction signals and circuits which combine these signals for proper overall correction.

Static Convergence Circuit

This circuit allows the customer to adjust static convergence (horizontal and vertical position of the red and blue rasters with respect to the green raster) via a subroutine in the VIDEO menu. Customer static convergence settings are stored in the system control EEPROM (U3200).

CIRCUIT OVERVIEW (Continued)

When the Convergence subroutine is employed, the system control micro (U3100) sends commands to the D/A converter (U8105). U8105 converts this data to four DC voltages (one each for red horizontal, red vertical, blue horizontal and blue vertical) which can be varied from 0 to 10 volts in 64 steps.

A quad op-amp (U8104) and a −5V regulator are used to shift the range of the D/A converter output so that step 32 (+5 volts) becomes 0 volts at the output of the op-amp, and the DC correction can vary above or below ground.

Dynamic Convergence Circuits

These circuits generate both horizontal- and vertical-rate signals which, when applied to the convergence yokes, adjust the size and shape of the individual rasters. The following signals are generated:

Vertical Sawtooth
Horizontal Sawtooth
Vertical Parabola
Horizontal Parabola
1/2 Horizontal Sawtooth
Vertical Sawtooth x Horizontal Sawtooth
1/2 Vertical Sawtooth x Horizontal Sawtooth
Vertical Sawtooth x Horizontal Parabola
1/2 Vertical Sawtooth x Horizontal Parabola
Vertical Parabola x Horizontal Sawtooth
Vertical Parabola x 1/2 Horizontal Sawtooth

When applied to the convergence yokes, these signals have the following effect on raster size and shape:

Signal	Correction
VSAW	Horizontal Skew
	Vertical Size
HSAW	Vertical Skew
	Horizontal Size
VPAR	Horizontal Bow
	Vertical Linearity
HPAR	Vertical Bow
	Horizontal Linearity
1/2 HSAW	Horizontal Linearity (Left Side)
VSAW x HSAW	Horizontal Keystone
	Vertical Keystone
1/2 VSAW x HSAW	Vertical Keystone (Bottom)
VSAW x HPAR	Vertical Pincushion
1/2 VSAW x HPAR	Vertical Pincushion (Bottom)
VPAR x HSAW	Horizontal Pincushion
VPAR x 1/2 HSAW	Horizontal Pincushion (Left Side)

Vertical Sawtooth Generator

A sawtooth waveform is developed across C8227 by charging the capacitor from the constant current source (Q8122) and discharging the capacitor through the reset switch (Q8121). Q8121 is reset (turned on) at a vertical rate by the vertical reset pulse from the one-chip (U1001 pin 29). This sawtooth waveform is buffered by Q8123 and Q8120 and sent to the convergence adjustment circuit to correct horizontal skew and vertical size.

Horizontal Sawtooth Generator

A sawtooth waveform is developed across C8130 by charging the capacitor from the constant current source (Q8107) and discharging the capacitor through the reset switch (Q8108). Q8108 is reset (turned on) at a horizontal rate by the filament pulse from the flyback (pin 5). This sawtooth waveform is buffered by Q8114 and Q8106 and sent to the convergence adjustment circuit to correct vertical skew and horizontal size.

Vertical Parabola Generator

The buffered sawtooth waveform at the emitter of Q8123 is fed to an inverting input of U8107, which integrates the sawtooth to obtain a parabolic waveform. To eliminate any DC offset in the parabola, the feedback capacitor (C8229) is discharged during retrace by the reset switch Q8138. The vertical parabola is buffered (Q8111) and clamped (Q8133) and sent to the convergence adjustment circuit to correct vertical linearity and horizontal bow.

Horizontal Parabola Generator

Two horizontal parabolas are generated, one of which (HPAR1) is used by the convergence modulators to develop additional correction waveforms. The other parabola (HPAR2) is fed directly to the convergence adjustment circuit.

In order to generate HPAR1, a sawtooth waveform is developed across C8236 by charging the capacitor from the current source (Q8136) and discharging the capacitor through the reset switch (Q8135). Q8135 is reset (turned on) at a horizontal rate by the filament pulse from the flyback (pin 5). Q8136 charge current is modified by the gull wing amp (Q8137) to give the sawtooth an "S" shaped correction. This sawtooth waveform is buffered by Q8128 and fed to an inverting input of U8107, which integrates the sawtooth to obtain a parabolic waveform. To eliminate any DC offset in the parabola, the feedback capacitor (C8231) is discharged during retrace by the reset switch Q8129.

HPAR2 is obtained by integrating the horizontal yoke current (T7001 and C8114). This parabola is clamped (Q8133) and sent to the convergence adjustment circuit to correct vertical bow and horizontal linearity.

1/2 Horizontal Sawtooth Generator

The buffered horizontal sawtooth at the emitter of Q8106 is AC coupled to Q8109 and Q8110, which clamp the signal so that only the negative-going portion of the signal remains. This correction signal is sent to the convergence adjustment circuit to correct horizontal linearity on the left side of the display.

Vertical Sawtooth x Horizontal Sawtooth Modulator

The buffered horizontal sawtooth from Q8106 and the buffered vertical sawtooth from Q8120 are combined in

CIRCUIT OVERVIEW (Continued)

U8103 to develop a horizontal sawtooth that is amplitude-modulated by a vertical sawtooth. This correction signal is buffered by Q8103 and sent to the convergence adjustment circuit to correct horizontal keystone and vertical keystone.

1/2 Vertical Sawtooth x Horizontal Sawtooth

The buffered vertical sawtooth from Q8120 turns on Q8105 during the positive-voltage half of the vertical sawtooth, causing the first half of the VSAW x HSAW waveform from Q8103 to be shorted to ground. This correction signal is buffered by Q8104 and sent to the convergence adjustment circuit to correct vertical keystone at the bottom of the display.

Vertical Sawtooth x Horizontal Parabola Modulator

The horizontal parabola from U8107 and the buffered vertical sawtooth from Q8120 are combined in U8101 to develop a horizontal parabola that is amplitude-modulated by a vertical sawtooth. This correction signal is buffered by Q8101 and sent to the convergence adjustment circuit to correct vertical pincushion.

1/2 Vertical Sawtooth x Horizontal Parabola

The buffered vertical sawtooth from Q8120 turns on Q8117 during the positive-voltage half of the vertical sawtooth, causing the first half of the VSAW x HPAR waveform from Q8101 to be shorted to ground. This correction signal is buffered by Q8104 and sent to the convergence adjustment circuit to correct vertical pincushion at the bottom of the display.

Vertical Parabola x Horizontal Sawtooth Modulator

The buffered horizontal sawtooth from Q8106 and the buffered vertical parabola from Q8111 are combined in U8102 to develop a horizontal sawtooth that is amplitude-modulated by a vertical parabola. This correction signal is buffered by Q8102 and sent to the convergence adjustment circuit to correct horizontal pincushion. R8193 is adjusted to obtain a symmetrical waveform.

Vertical Parabola x 1/2 Horizontal Sawtooth

The buffered VPAR x HSAW signal from Q8102 is AC coupled to Q8112 and Q8113, which clamp the signal so that only the negative-going portion of the signal remains. This correction signal is sent to the convergence adjustment circuit to correct horizontal pincushion on the left side of the display.

Convergence Adjustment Circuit

The dynamic correction signals described above are sent to a set of variable resistors where the signals are combined and routed to summing amplifiers (U8201, U8202 and U8203). Each variable resistor is connected in a divider network and connected to the inverting and noninverting inputs of the summer so that the amount and direction of the correction can be adjusted. Since the static correction signals are adjusted via software in the system control menu and can be either adjusted either positive or negative, each of these correction signals is connected directly to one input of a summer. The six outputs from the summer amplifiers are sent to the convergence output amplifiers on the PTV Auxiliary board to drive the convergence yokes.

Convergence Output Amplifier

The convergence output amplifiers convert the convergence correction signal from a voltage waveform to a current waveform suitable for driving the convergence yoke coils. There are six amplifiers - one each for red horizontal correction, red vertical correction, green horizontal correction, green vertical correction, blue horizontal correction and blue vertical correction. All of the amplifiers use an emitter follower push-pull output stage that uses ±15V supplies. The vertical amplifiers use additional output devices (top and bottom boost, which use ±45V supplies) in order to provide a large output voltage swing for fast retrace. The red and blue horizontal amplifiers use only a top boost device and the green horizontal amplifier requires no boost.

Red Vertical Amplifier

The convergence correction voltage is applied to the inverting input of error amp U7002 and the resulting error voltage is fed to Q7019. Since the base of Q7019 is at a fixed voltage reference, so is its emitter. As the error voltage at the output of the error amp changes, the current through Q7019 changes. Since the base of Q7020 is at a fixed voltage reference (CR7065 and CR7066), so is its emitter. This results in a constant current through R7069 that is divided between Q7019 and Q7020. As the current through Q7019 changes, so does the current through Q7020, and this current flows through CR7028, CR7029, CR7030 and R7071 to drive the output devices.

During scan, output current is provided by the ±15V supplies through R7074 and R7083. However, some of the correction signals require large changes in output current during retrace. To obtain fast current changes during retrace, the boost transistors (Q7021 and Q7024) are turned on to supply ±45V to the output transistors. As the output voltage increases towards +15V, the voltage at the base of Q7021 increases (via CR7033) until it is turned on, supplying +45V to Q7022. Similarly, as the output voltage decreases towards −15V, the voltage at the base of Q7024 decreases (via CR7036) until it is turned on, supplying −45V to Q7022.

Green and Blue Vertical Amplifiers

The green and blue vertical amplifiers function in a manner similar to the red vertical amplifier.

Red and Blue Horizontal Amplifiers

The red and blue horizontal amplifiers function in a manner similar to the red vertical amplifier, except that the signals used for horizontal correction are such that −45V supply boost is not required.

Green Horizontal Amplifier

The green horizontal amplifier functions in a manner similar to the red vertical amplifier, except that the signals used for horizontal correction are such that neither −45V nor +45V supply boost is required.